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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/416,501	10/08/1999	BRIAN S. DOYLE	42390.P4514D	6248

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EXAMINER
ORTIZ, EDGARDO

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/416,501	Doyle
Examiner	**Art Unit**
Edgardo Ortiz	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Feb 11, 2002*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *28-32* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *28-32* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
18) ☐ Interview Summary (PTO-413) Paper No(s). _____
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

This Office Action is in response to an amendment filed February 11, 2002 on which Applicant canceled claims 14 and 22-27 and added new claims 28-32.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 28-30 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Sakaguchi et.al. (U.S. Patent No. 5,966,620) in view of Applicant's acknowledged prior art figure 2 and the description thereof of pages 3-4 of the instant application disclosure. With regard to Claim 28, Sakaguchi teaches a first single crystal substrate portion (11) having a dielectric layer (13) on a surface and a second substrate (15) portion formed thereon, wherein the dielectric layer of the first substrate portion is bonded to the surface of the second substrate portion.

However, Sakaguchi fails to teach that the second substrate portion has devices formed thereon and defines a device surface. Applicant's admitted prior art figure 2 teaches a primary substrate (202) having a first level of devices (204) formed thereon and defining a device surface and at least a secondary substrate (Si) coupled to the device surface. Therefore, it would have been an

obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Sakaguchi to include a second substrate portion having devices formed thereon and defining a device surface, as suggested by pages 3-4 of the instant application disclosure describing the prior art, in order to improve the integration and bonding of semiconductor layers including transistors.

Additionally, the claim contains the limitation "the first substrate portion formed of less than an entire portion of a starting material by demarcating a film thickness through ion implantation into the starting material and separating the first substrate portion from the starting material". It is noted that this is a product by process limitation. A "product by process" claim is directed to the product per se, no matter how actually made, In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

With regard to Claim 29, a further difference between the claimed invention and Sakaguchi is, a plurality of devices formed on the first substrate portion. Applicant's admitted prior art figure 2 teaches a primary substrate (202) having a first level of devices (204) formed thereon and defining a device surface. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Sakaguchi to include a plurality of devices formed on the first substrate portion, as suggested by pages 3-4 of the instant application disclosure describing the prior art, in order to improve integration of semiconductor devices, such as transistors, into a single substrate layer.

With regard to Claim 30, a further difference between the claimed invention and Sakaguchi is, selected ones of the devices of the first substrate portion and selected ones of the devices of the second substrate portion that are interconnected. Applicant's admitted prior art figure 2 teaches selected ones of the first level of devices (204) of the primary substrate (202) and selected ones of the devices (208) of the secondary substrate (Si) that are interconnected. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Sakaguchi to include selected ones of the devices of the first substrate portion and selected ones of the devices of the second substrate portion that are interconnected, as suggested by pages 3-4 of the instant application disclosure describing the prior art, in order to improve the integration and bonding of semiconductor layers including transistors.

Claims 31 and 32 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Applicant's acknowledged prior art figure 2 and the description thereof of pages 3-4 of the instant application disclosure. With regard to Claim 31, Applicant's admitted prior art figure 2 teaches a primary substrate (202) having a first level of devices (204) formed thereon and defining a device surface and at least a secondary substrate (Si) coupled to the device surface, the at least one secondary substrate having devices (208) formed thereon.

However, Applicant's admitted prior art figure 2 fails to teach that the secondary substrate is of the single-crystal kind. As disclosed on page 4, providing a second layer of transistors made of single crystal silicon has been known in the art. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Applicant's admitted prior art figure 2 to include a secondary substrate of the single-crystal kind, as suggested by pages 3-4 of the instant application disclosure describing the prior art, in order to provide a crystalline material with long range order throughout as the substrate material.

With regard to Claim 32, Applicant's admitted prior art figure 2 teaches selected ones of the first level of devices (204) of the primary substrate (202) and selected ones of the devices (208) of the secondary substrate (Si) that are interconnected.

Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Edgardo Ortiz (Art Unit 2815), whose telephone number is (703) 308-6183 or by fax at (703) 308-7722. In case the Examiner can not be reached, you might call Supervisor Eddie Lee at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 receptionist whose telephone number is (703) 308-0956.

EO/AU 2815

2/23/02

EDDIE LEE
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